UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,894	10/26/2001	John Erik Lindholm	NVID-045/01US 140060-2084	7963

23419 7590 03/30/2009

COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
Washington, DC 20001

EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
03/30/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN ERIK LINDHOLM and SIMON MOY

Appeal 2009-0966
Application 10/032,894
Technology Center 2600

Decided:[1] March 30, 2009

Before MAHSHID D. SAADAT, ROBERT E. NAPPI,
and MARC S. HOFF, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 24, 25, and 27-34. Claims 1-23, 26, and 35-41 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention relates generally to graphics processors and, more specifically, to a lighting module of a graphics pipeline system (Spec. 1). According to Appellants, the output of the lighting module is the screen space data suitable for setting up primitives, which are used in the rasterization module for generating the output data (Spec. 11).

Independent claims 24 and 30 are representative and read as follows:

24. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a register unit coupled to the arithmetic logic unit; and

(e) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit;

wherein the lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

30. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom;

(b) a multiplication logic unit coupled to the at least one input buffer;

(c) an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit;

(d) a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit; and

(e) memory coupled to the multiplication logic unit and the arithmetic logic unit;

wherein the multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit.

The Examiner relies on the following prior art reference:

Krech	US 6,184,902 B1	Feb. 6, 2001 (filed Apr. 30, 1997)

Claims 24, 25, and 27-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Krech.

Rather than reiterate the arguments of Appellants and the Examiner, we refer to the Briefs (Appeal Brief re-filed Mar. 6, 2007 and Reply Brief filed Nov. 22, 2005) and the Answer (mailed May 9, 2007) for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants did not make in the Briefs have not been considered and are deemed waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The issue is whether the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e). With respect to independent claim 24, the issue specifically turns on whether Krech discloses coupling a lighting logic unit to a multiplication logic unit through a conversion module. With respect to independent claims 30 and 34, the issue is specifically whether Krech discloses a multiplication logic unit with a feedback loop coupled to an input of the multiplication logic unit.

PRINCIPLES OF LAW

1. Anticipation

A rejection for anticipation requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. *See Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

2. Burdens of Proof and Production

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). Only if that burden is met does the burden of going forward shift to the applicant. *In re King*, 801 F.2d 1324, 1327 (Fed. Cir. 1986); *In re Wilder*, 429 F.2d 447, 450 (CCPA 1970).

Once a prima facie case is established and rebuttal evidence is submitted, the ultimate question becomes whether, based on the totality of

the record, the examiner carried his burden of proof by preponderance. *See Oetiker*, 977 F.2d at 1445. If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. *Fine*, 837 F.2d at 1074.

ANALYSIS

With respect to independent claim 24, the Examiner refers to the components depicted in Figure 5 of Krech and reads the claimed "multiplication unit" on multiplier 55, the claimed "lighting logic" on control logic element 115, and the claimed "conversion module" on element 17 (Ans. 3 and 6-7). The Examiner further relies on column 11, line 45 through column 13, line 15 of Krech for describing the transform mechanism of light conversion and grouping of vertices/lights in the control unit 17 (Ans. 7-8).

Appellants assert that Krech does not disclose coupling a lighting logic unit and a multiplication logic unit through a conversion module (App. Br. 5). In particular, Appellants disagree (Reply Br. 4-5) with the Examiner's characterization of branch central intelligence 112, state management address decode 132, vertex/light counter 139, or control logic element 115 in Figure 5 of Krech as the claimed "lighting logic unit" because these elements carry lighting logic. Appellants argue that the Examiner's reasoning implies that even a mere conductor carrying lighting logic would disclose a lighting logic unit, whereas, while the lighting logic units are known in the art, the claimed unit and its relationship to other components are not (Reply Br. 5).

Based on a review of the reference, we remain unpersuaded by Appellants' argument that the Examiner unreasonably read the claimed lighting logic unit on the elements identified in the embodiment depicted in Figure 5 of Krech. We specifically find that Figure 5 shows that state data 133 from input buffer 77 is received in state management address decode 132 (col. 8, ll. 13-18), then sent to branch central intelligence 112 via mode information 134 (col. 8, ll. 34-37), and finally directed to individual control unit logic elements 115 via signal 138 (col. 8, ll. 42-48). We also find that the Examiner's characterization of control unit logic elements 115 in Figure 5 of Krech as the claimed lighting logic units (Ans. 9) to be reasonable since Krech describes processing in those units the light data counted by counter 139 via the last light bit 137 (col. 13, ll. 9-15).

Similarly, we find that the Examiner has reasonably equated (Ans. 8) the claimed conversion module with the control unit 17 in ROM 100, where all vertices and all lights are processed (col. 12, ll. 22-31) after they are received from logic element 115 via MUX 146 and latch 149 (col. 10, ll. 9-27). The conversion module functionalities in ROM 100, as described in the flow charts of Figures 7A-7C and the corresponding text (col. 10, l. 28 – col. 12, l. 20), and explained by the Examiner (Ans. 9), include TRANSFORM, DECOMP, CLIP, etc., which represent the transformation on the vertex data. Therefore, we find that the Examiner has satisfied the initial burden of setting forth a prima facie case of anticipation by identifying the recited elements of claim 24 in the disclosure of Krech. However, for the reasons discussed above, we do not find Appellants' arguments and general allegations of patentability to be sufficient to rebut the Examiner's prima facie case.

With respect to the feedback loop coupled to an input of the multiplication logic unit, as recited in claim 30, Appellants argue (App. Br. 6-8) that Figure 5 of Krech does not show any type of feedback loop. We again find the Examiner's position to be reasonable. In particular, we agree with the Examiner's findings that the cited portions of Krech and Figure 5 show a feedback loop corresponding to the multiplication logic unit 55 through lines 131 (FLGS) to logic element 115, lines 148 to MUX 146, lines 151 to latch 149, lines 108 to ROM 100, and lines 125 back to the multiplication logic unit 55. We further disagree with Appellants (Reply Br. 6) that the collection of lines 131-125 is not coupled to the input of Krech's multiplier 55. In that regard, Krech specifically discloses that lines 131 and 125 are output and input lines connected to the processing elements in stack 51, including multiplier 55 (col. 8, ll. 4-8 and col. 14, ll. 16-19).

CONCLUSION

Appellants present no specific arguments for claims 25, 27-29, and 31-34 and argue their patentability based on the same arguments made *supra* with respect to claims 24 and 30 (App. Br. 8). As discussed above, we find that the Examiner has satisfied the initial burden of setting forth a prima facie case by relying on Krech's teachings related to multiplier 55, logic unit 115, and conversion module 17, which Appellants have not successfully rebutted. In view of the above discussions, since Appellants have not shown any error in the Examiner's position and all of the claimed limitations are shown to be present in the disclosure of Krech, the Examiner's 35 U.S.C. § 102(e) rejection of independent claims 24 and 30, as well as claims 25, 27-29, and 31-34, is sustained.

ORDER

The decision of the Examiner rejecting claims 24, 25, and 27-34 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

babc

COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
Suite 1100
777 - 6th Street, NW
Washington, DC 20001